

JEDEC STANDARD

Definition of the SSTUB32866 1.8 V Configurable Registered Buffer with Parity Test for DDR2 RDIMM Applications

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DEFINITION OF THE SSTUB32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-07-15, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUB32866 registered buffer with parity test for DDR2 RDIMM applications.

The purpose is to provide a standard for the SSTUB32866 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTUB32866 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity is designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control and reset ($\overline{\text{RESET}}$) inputs are LVCMOS. All data outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load, and meet SSTL_18 specifications. The error ($\overline{\text{QERR}}$) output is 1.8 V open-drain driver.

The SSTUB32866 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high, and $\overline{\text{CK}}$ going low.

The SSTUB32866 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D2–D3, D5–D6, D8–D25 when C0 = 0 and C1 = 0; D2–D3, D5–D6, D8–D14 when C0 = 0 and C1=1; or D1–D6, D8–D13 when C0 = 1 and C1=1) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent data inputs must be tied to a known logic state.

When used as a single device, the C0 and C1 inputs are tied low. In this configuration, parity is checked on the PAR_IN input which arrives one cycle after the input data to which it applies. Two cycles after the data are registered, the corresponding partial-parity-out (PPO) and $\overline{\text{QERR}}$ signals are generated.

2.1 Description (cont'd)

When used in pairs, the C0 input of the first register is tied low and the C0 input of the second register is tied high. The C1 input of both registers are tied high. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the first device. Two clock cycles after the data are registered the corresponding PPO and $\overline{\text{QERR}}$ signals are produced on the second device. The PPO output of the first register is cascaded to the PAR_IN of the second register. The $\overline{\text{QERR}}$ output of the first register is left floating and the valid error information is latched on the $\overline{\text{QERR}}$ output of the second register.

If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched as low for a clock duration equal to the parity-error duration or until $\overline{\text{RESET}}$ is driven low. For the case where a parity error occurs just before the device enters the low-power mode (LPM), see Table 4, Figure 18, Figure 19, and Figure 20. The DIMM-dependent signals ($\overline{\text{DCKE}}$, $\overline{\text{DCS}}$, $\overline{\text{DODT}}$, and $\overline{\text{CSR}}$) are not included in the parity check computation. The parity error output $\overline{\text{QERR}}$ will be reset to high by $\overline{\text{RESET}}$ transitioning low and will not be decoded until after $\overline{\text{RESET}}$ goes high and $\overline{\text{DCS}}$ and/or $\overline{\text{CSR}}$ are asserted low.

The C0 input controls the pinout configuration for the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the Qn outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTUB32866 must ensure that the outputs will remain low, thus ensuring no glitches on the output. If the data inputs are not held low, then $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ must be held high, $\overline{\text{DODT}}$ and $\overline{\text{DCKE}}$ must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{\text{RESET}}$.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$, C0, and C1 inputs must always be held at a valid logic high or low level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS}}$ and $\overline{\text{CSR}}$) inputs and will gate the Qn and PPO outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is low, the Qn and PPO outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and when driven low will force the Qn and PPO outputs low, and the $\overline{\text{QERR}}$ output high. If the $\overline{\text{DCS}}$ control functionality is not desired, then the $\overline{\text{CSR}}$ input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{\text{DCS}}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS}}$ only, then the $\overline{\text{CSR}}$ input should be pulled up to V_{DD} through a pullup resistor.

Package options include 96-ball LFBGA (MO-205CC).

2.2 96-ball LFBGA (MO-205CC)

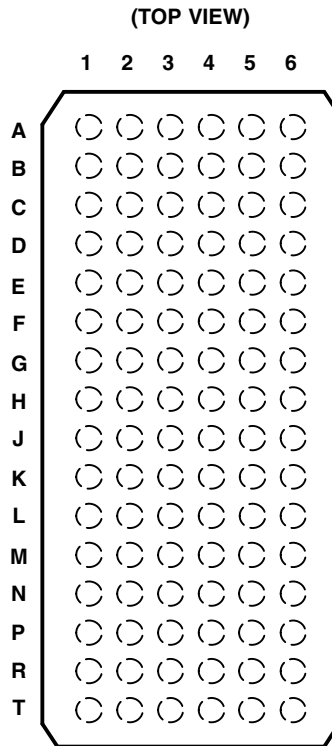


Figure 1 — Pinout Configuration

2.3 Pinout Top View for 96-ball LFBGA

A	DCKE	PPO	V _{REF}	V _{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V _{DD}	V _{DD}	Q3	Q16
D	DODT	$\overline{\text{QERR}}$	GND	GND	QODT	DNU
E	D5	D17	V _{DD}	V _{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	$\overline{\text{RESET}}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$	DNU
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V _{DD}	V _{DD}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V _{DD}	V _{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V _{DD}	V _{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V _{DD}	V _{DD}	Q13	Q24
T	D14	D25	V _{REF}	V _{DD}	Q14	Q25
	1	2	3	4	5	6

Figure 2 — 1:1 Register (C0=0, C1=0)

2.3 Pinout Top View for 96-ball LFBGA (cont'd)

A	DCKE	PPO	V _{REF}	V _{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	DODT	\overline{QERR}	GND	GND	QODTA	QODTB
E	D5	NC	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	PAR_IN	\overline{RESET}	V _{DD}	V _{DD}	C1	C0
H	CK	\overline{DCS}	GND	GND	\overline{QCSA}	\overline{QCSB}
J	\overline{CK}	\overline{CSR}	V _{DD}	V _{DD}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V _{DD}	V _{DD}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	D14	DNU	V _{REF}	V _{DD}	Q14A	Q14B
	1	2	3	4	5	6

Figure 3 — 1:2 Register A (C0=0, C1=1)

A	D1	PPO	V _{REF}	V _{DD}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	D4	\overline{QERR}	GND	GND	Q4A	Q4B
E	D5	DNU	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	\overline{RESET}	V _{DD}	V _{DD}	C1	C0
H	CK	\overline{DCS}	GND	GND	\overline{QCSA}	\overline{QCSB}
J	\overline{CK}	\overline{CSR}	V _{DD}	V _{DD}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	V _{DD}	V _{DD}	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	DCKE	DNU	V _{REF}	V _{DD}	QCKEA	QCKEB
	1	2	3	4	5	6

Figure 4 — 1:2 Register B (C0=1, C1=1)

NOTE DNU denotes do not use. NC denotes no internal connection.

2.4 Terminal Functions

Table 1 — Terminal Functions

Terminal name	Description	Electrical characteristics
GND	Ground	Ground input
V _{DD}	Power supply voltage	1.8-V nominal
V _{REF}	Input reference voltage	0.9-V nominal
CK	Positive main clock input	Differential input
$\overline{\text{CK}}$	Negative main clock input	Differential input
C0, C1	Configuration control inputs - Register A or Register B and 1:1 mode or 1:2 mode select	LVC MOS inputs
$\overline{\text{RESET}}$	Asynchronous reset input – resets registers and disables V _{REF} data and clock differential-input receivers. When $\overline{\text{RESET}}$ is low all Q outputs are forced low and $\overline{\text{QERR}}$ output is forced high.	LVC MOS input
$\overline{\text{CSR}}$, $\overline{\text{DCS}}$	Chip select inputs – disables D1-D24† outputs switching when both inputs are high	SSTL ₁₈ input
D1–D25	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{\text{CK}}$	SSTL ₁₈ input
DODT	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL ₁₈ input
DCKE	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL ₁₈ input
PAR_IN	Parity input - arrives one clock cycle after the corresponding data input.	SSTL ₁₈ input
Q1–Q25 ²	Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS outputs
PPO	Partial parity out - indicates odd parity of inputs D1 - D25 ¹	1.8-V CMOS output
$\overline{\text{QCS}}$	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS output
QODT	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS output
QCKE	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8-V CMOS output
$\overline{\text{QERR}}$	Output error bit - Timing is determined by the device mode.	Open-drain output
NC	No internal connection	
DNU	Do not use - inputs are in standby-equivalent mode and outputs are driven low.	
<p>NOTE 1 Data inputs = D2, D3, D5, D6, D8-D25 when C0=0 and C1=0 Data inputs = D2, D3, D5, D6, D8-D14 when C0=0 and C1=1 Data inputs = D1-D6, D8-D10, D12, D13 when C0=1 and C1=1</p> <p>NOTE 2 Data outputs = Q2, Q3, Q5, Q6, Q8-Q25 when C0=0 and C1=0 Data outputs = Q2, Q3, Q5, Q6, Q8-Q14 when C0=0 and C1=1 Data outputs = Q1-Q6, Q8-Q10, Q12, Q13 when C0=1 and C1=1</p>		

2.5 Function Table

Table 2 — Function Table (Each Flip Flop)

Inputs						Outputs		
$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CK	$\overline{\text{CK}}$	Dn, DODTn, DCKEn	Qn	$\overline{\text{QCS}}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	H	↑	↓	L	Q_0	H	L
H	H	H	↑	↓	H	Q_0	H	H
H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

Input-Data Error Occurrence ²	1:1 Mode (C0=0, C1=0)		1:2 Register-A Mode (C0=0, C1=1)		1:2 Register-B Mode (C0=1, C1=1)	
	PPO Duration ^{3,4}	$\overline{\text{QERR}}$ Duration ³	PPO Duration ³	$\overline{\text{QERR}}$ Duration ^{3,4}	PPO Duration ^{3,4}	$\overline{\text{QERR}}$ Duration ³
n-2	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles
n-1	2 Cycles after LPM is de-asserted	2 Cycles after LPM is de-asserted	1 Cycles after LPM is de-asserted	1 Cycles after LPM is de-asserted	2 Cycles after LPM is de-asserted	2 Cycles after LPM is de-asserted
n	Not detected	Not detected	Not detected	Not detected	Not detected	Not detected

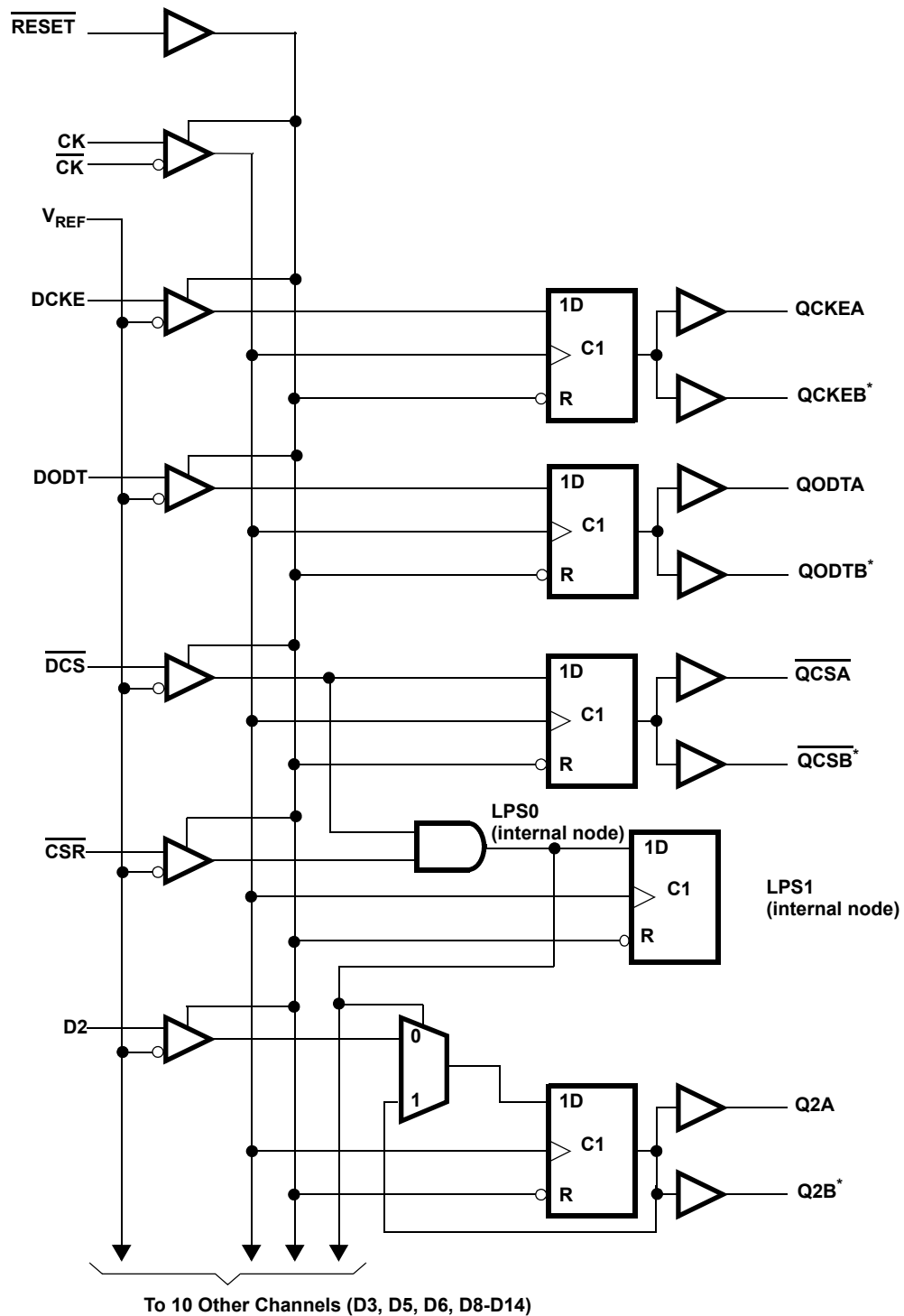
NOTE 1 If a parity error occurs before the device enters the low-power mode (LPM), the behavior of PPO and $\overline{\text{QERR}}$ is dependent on the mode of the device and the position of the parity error occurrence. This table illustrates the low-power-mode effect on parity detect. The low-power mode is activated on the n clock cycle when DCS and CSR go high.

NOTE 2 The clock-edge position of a one-cycle data-input error relative to the clock-edge (n) which initiates LPM at the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs.

NOTE 3 If an error occurs, the PPO output may be driven high and the $\overline{\text{QERR}}$ output driven low. These columns show the clock duration for which the PPO signal will be held high or the $\overline{\text{QERR}}$ signal will be held low.

NOTE 4 Not used.

2.6 Logic Diagram



* Disabled in 1:1 configuration

Figure 5 — Logic Diagram 1:2 Register-A Configuration with C0=0 and C1=1 (Positive Logic)

2.6 Logic Diagram (cont'd)

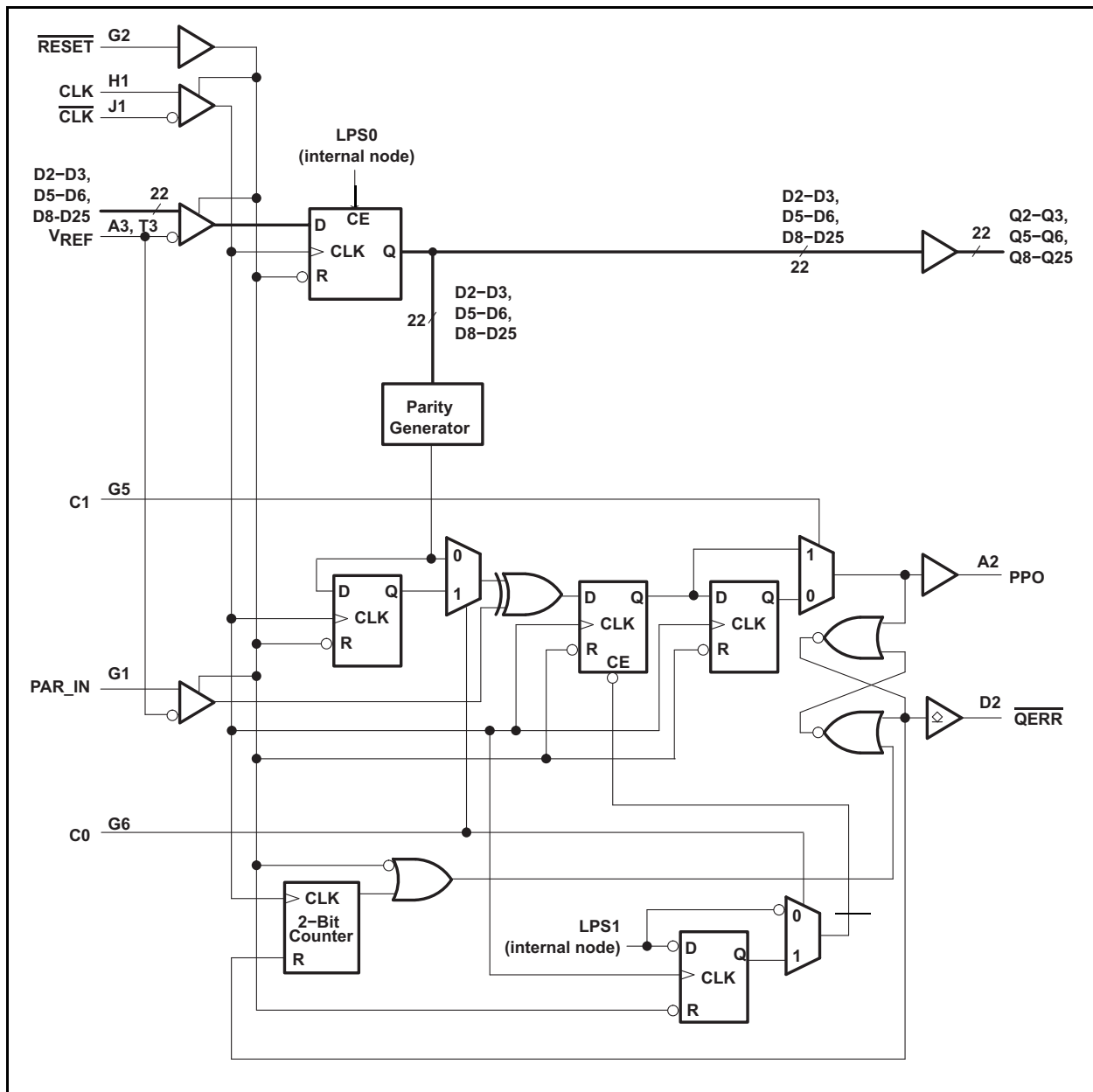


Figure 6 — Parity Logic Diagram for 1:1 Register Configuration (Positive Logic); C0=0, C1=0

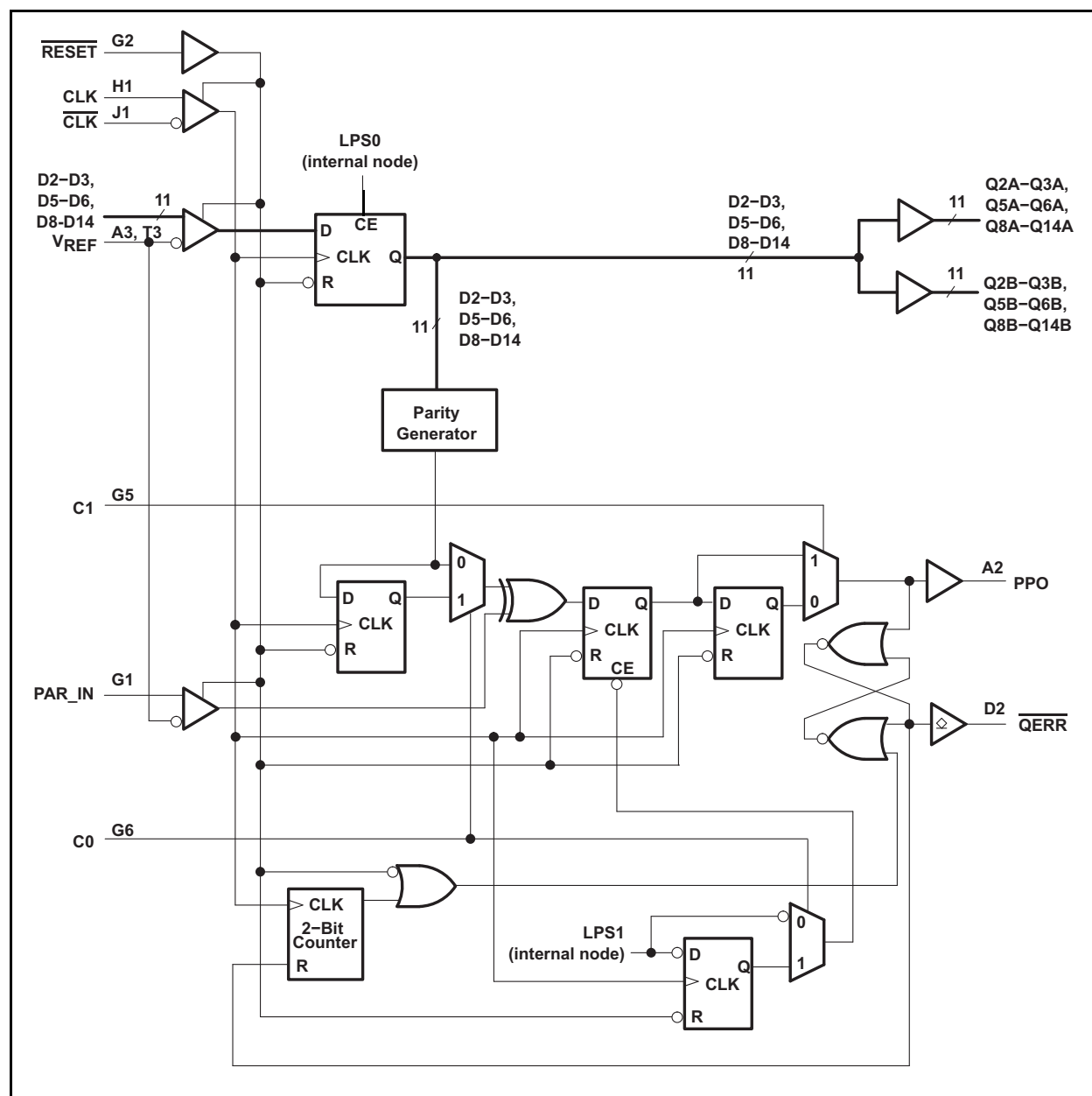


Figure 7 — Parity Logic Diagram for 1:2 Register-A Configuration (Positive Logic); C0=0, C1=1

2.6 Logic Diagram (cont'd)

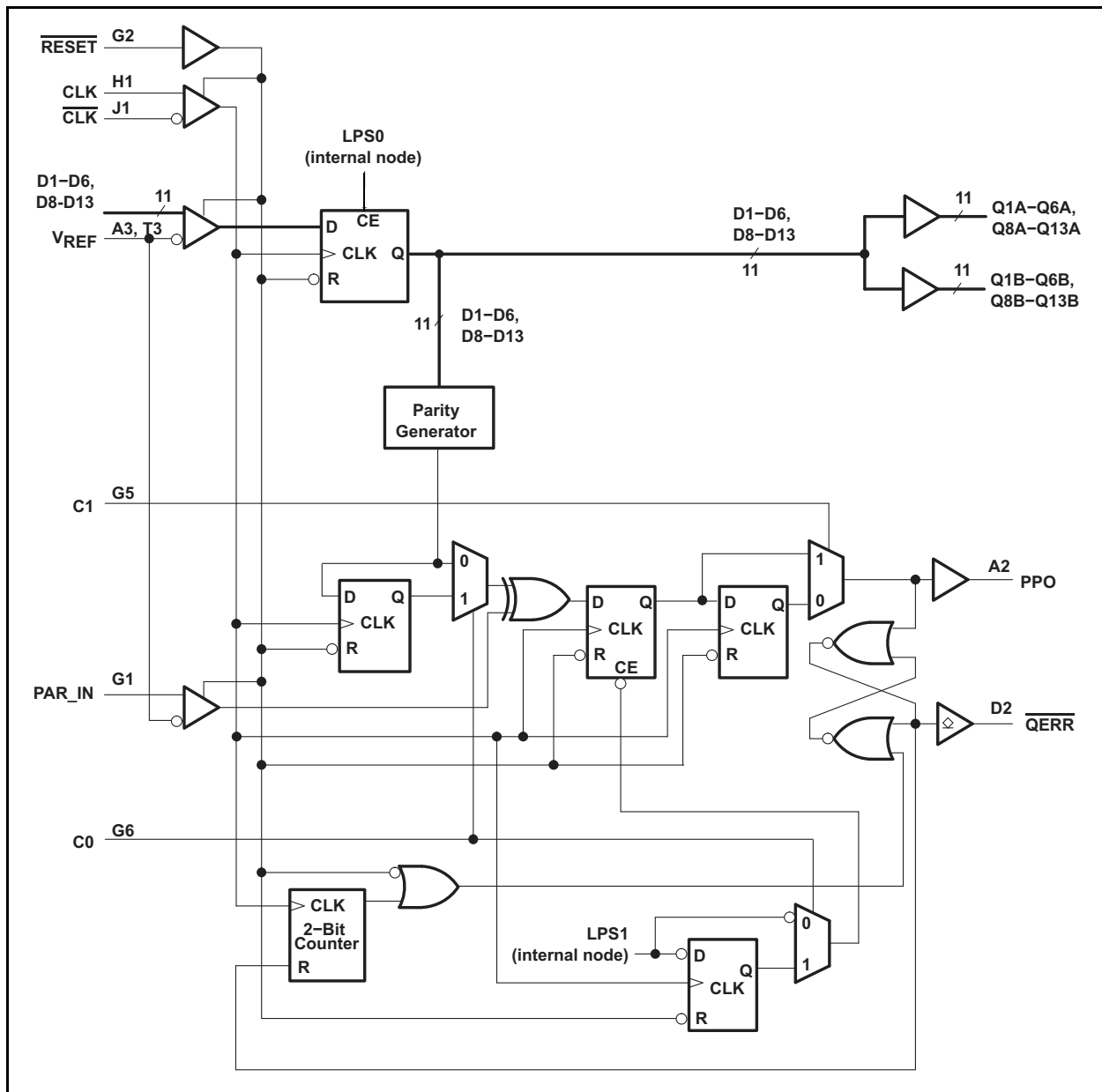
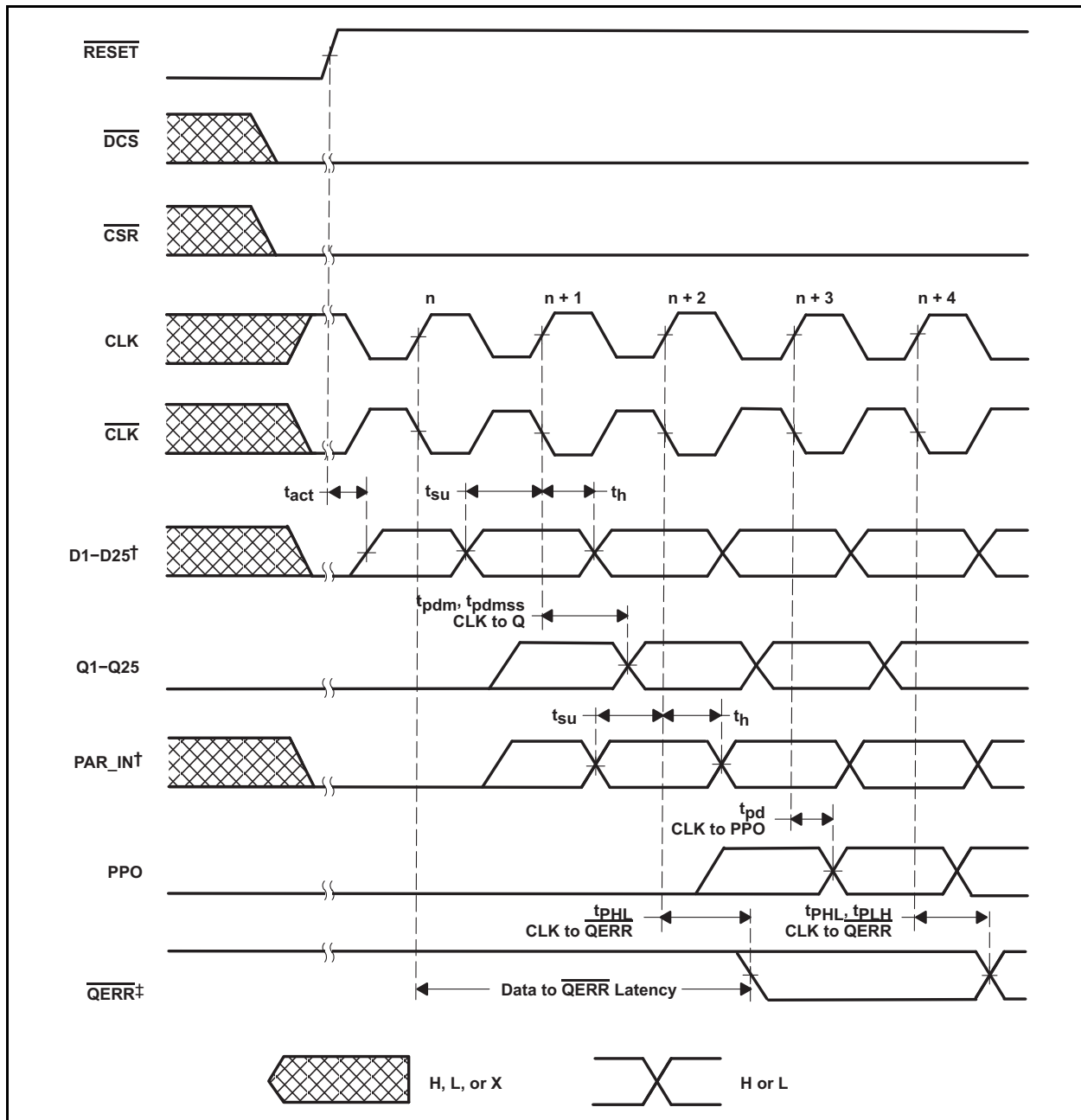


Figure 8 — Parity Logic Diagram for 1:2 Register-B Configuration (Positive Logic); C0=1, C1=1

2.7 Register Timing



**Figure 9 — Timing Diagram for SSTUB32866 Used as a Single Device; C0=0, C1=0;
RESET Switches from L to H**

† After $\overline{\text{RESET}}$ is switched from low to high, if $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ are held Low than all data and PAR_IN input signals must be held Low for a minimum time of $t_{\text{ACT max}}$ to avoid false error. If $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ are held high than all data and PAR_IN inputs signals must be held at valid logic levels for a minimum time of $t_{\text{ACT max}}$, to avoid false error.

‡ If the data is clocked in on the n clock pulse, and PAR_IN is clocked in at $n+1$, the $\overline{\text{QERR}}$ output signal will be generated on the $n+2$ clock pulse, and it will be valid on the $n+3$ clock pulse.

2.7 Register Timing (cont'd)

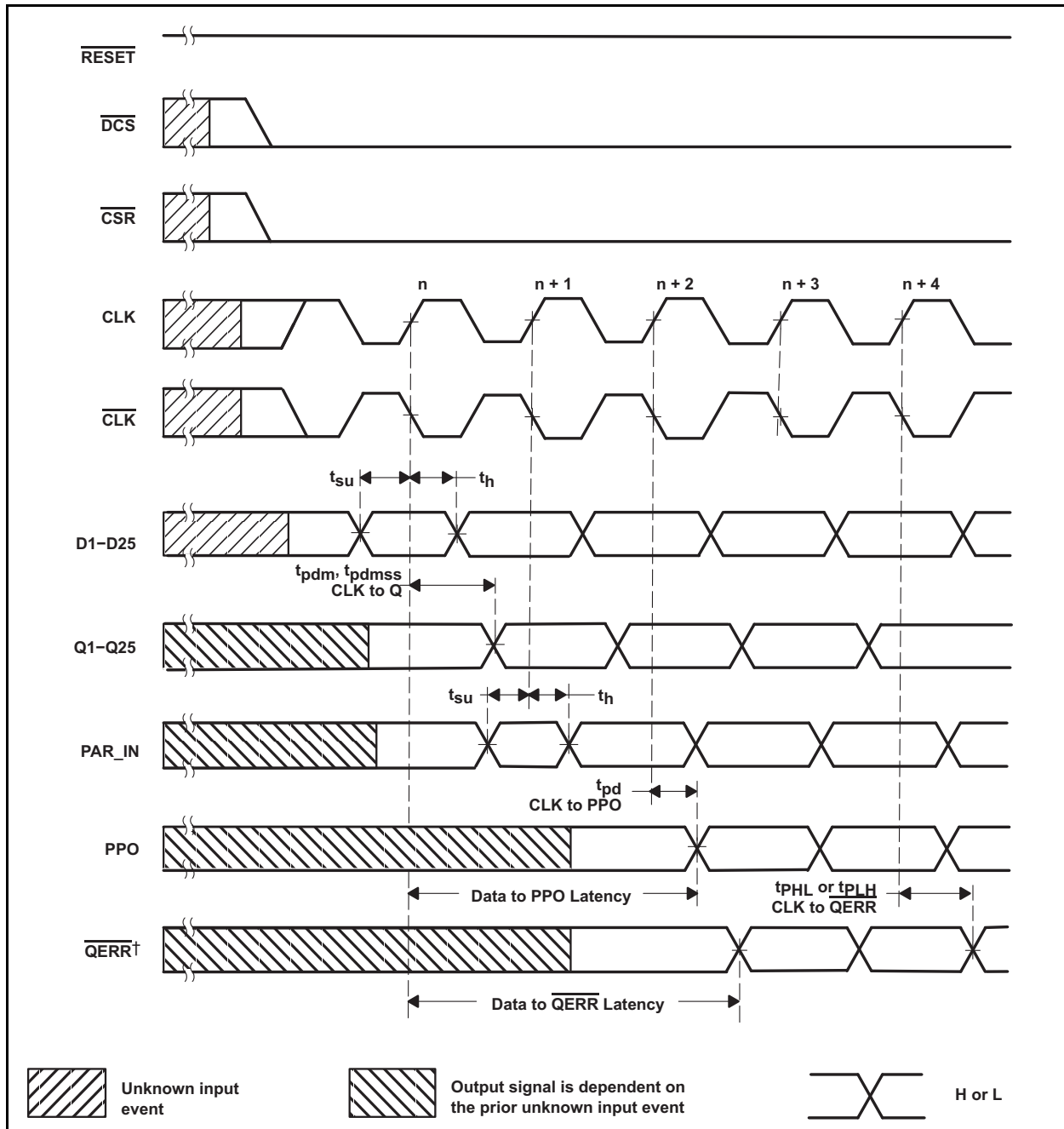


Figure 10 — Timing Diagram for SSTUB32866 Used as a Single Device; C0=0, C1=0; RESET Being Held HIGH

†

If the data is clocked in on the n clock pulse, and $\overline{\text{PAR_IN}}$ is clocked in at $n+1$, the $\overline{\text{QERR}}$ output signal will be generated on the $n+2$ clock pulse, and it will be valid on the $n+3$ clock pulse. If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low.

2.7 Register Timing (cont'd)

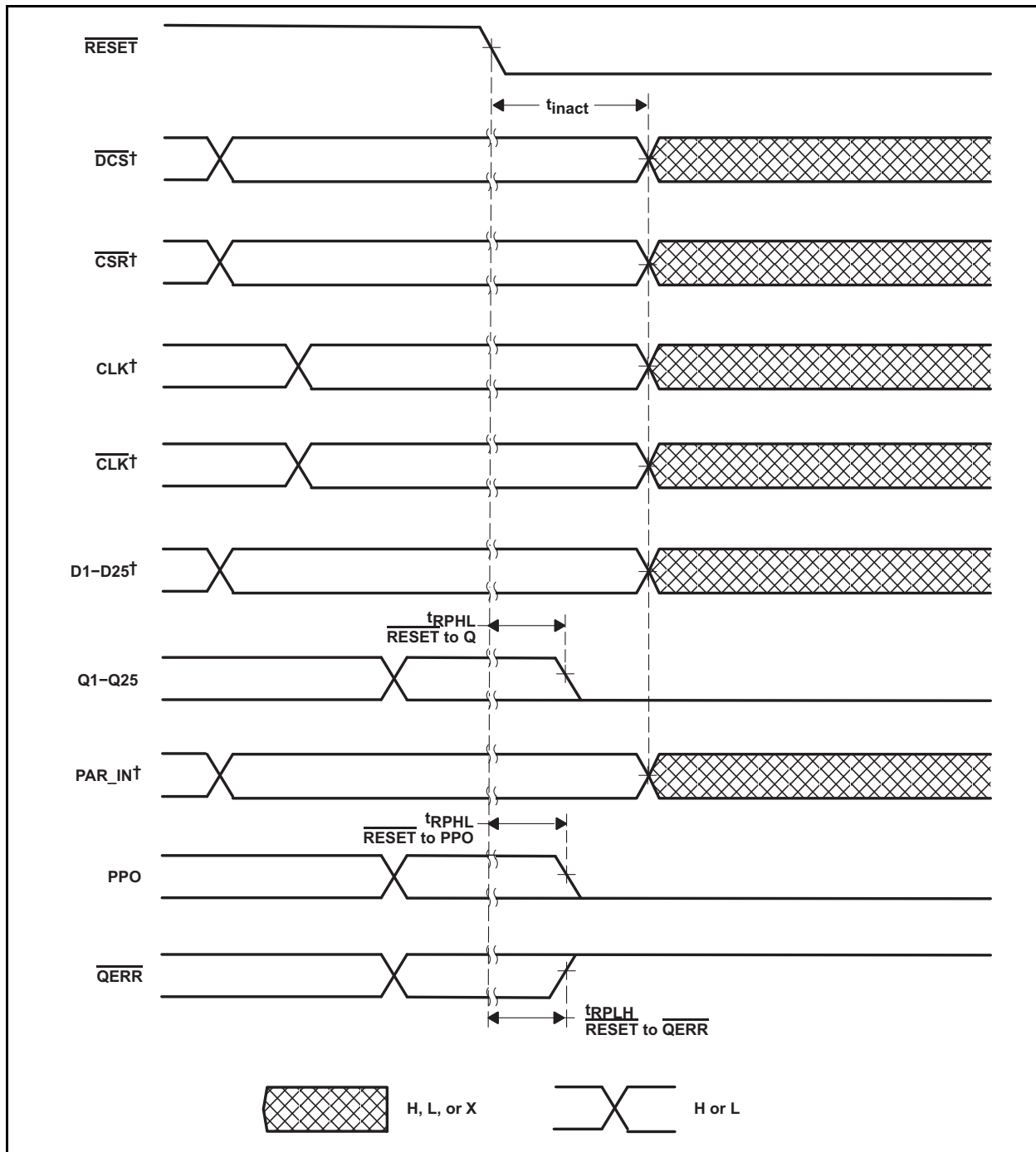


Figure 11 — Timing Diagram for SSTUB32866 Used as a Single Device; C0=0, C1=0; RESET Switches from H to L

†

After $\overline{\text{RESET}}$ is switched from high to low, all data and clock inputs signals must be set and held at valid logic levels (not floating) for a minimum time of $t_{INACT\ max}$

The diagram shows the timing of various signals relative to the clock (CLK) and data bus (D1-D14). Key timing parameters include:

- t_{act} : Activation time for D1-D14.
- t_{su} : Setup time for D1-D14 relative to CLK.
- t_h : Hold time for D1-D14 relative to CLK.
- t_{pdm}, t_{pdmss} : Delay from CLK to Q for D1-D14.
- t_{su} : Setup time for Q1-Q14 relative to CLK.
- t_h : Hold time for Q1-Q14 relative to CLK.
- t_{pd} : Delay from CLK to PPO.
- t_{PHL}, t_{PLH} : Delay from CLK to QERR.
- t_{QERR} : Delay from Data to QERR Latency.

Legend:

- Hatched area: H, L, or X
- Crossing line: H or L

† After **RESET** is switched from low to high, if **DCS0** or **DCS1** are held Low than all data and **PAR_IN** input signals must be held Low for a minimum time of $t_{ACT\ max}$ to avoid false error. If **DCS0** or **DCS1** are held high than all data and **PAR_IN** inputs signals must be held at valid logic levels for a minimum time of $t_{ACT\ max}$, to avoid false error.

† If the data is clocked in on the n clock pulse, and PAR_IN is clocked in at n+1, the $\overline{\text{QERR}}$ output signal will be generated on the n+1 clock pulse, and it will be valid on the n+2 clock pulse.

2.7 Register Timing (cont'd)

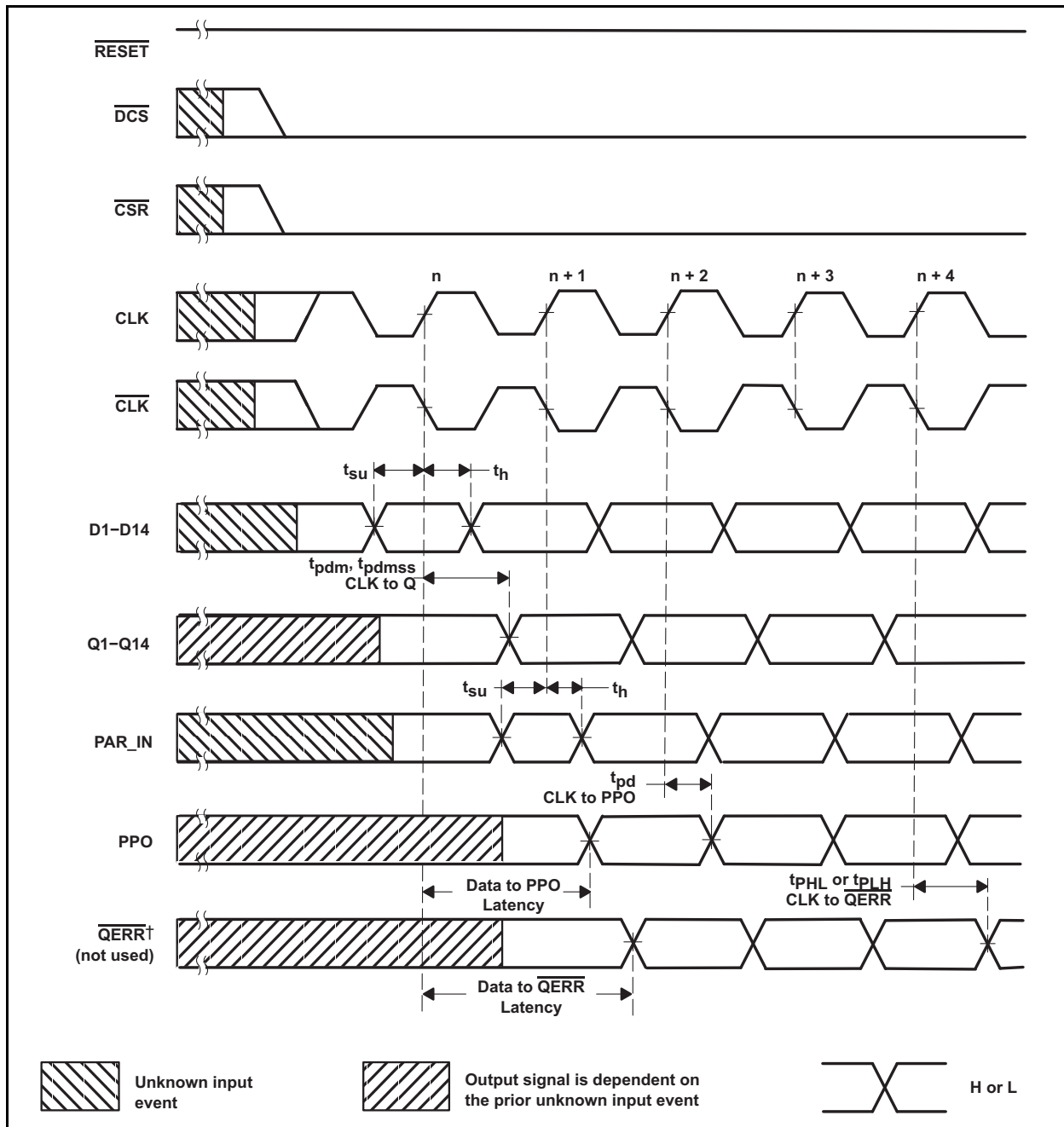


Figure 13 — Timing Diagram for the First SSTUB32866 (1:2 Register-A Configuration) Device Used in Pair; C0 = 0, C1 = 1; RESET Being Held HIGH

† If the data is clocked in on the n clock pulse, and PAR_IN is clocked in at n+1, the \overline{QERR} output signal will be generated on the n+1 clock pulse, and it will be valid on the n+2 clock pulse. If an error occurs and the \overline{QERR} output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low.

2.7 Register Timing (cont'd)

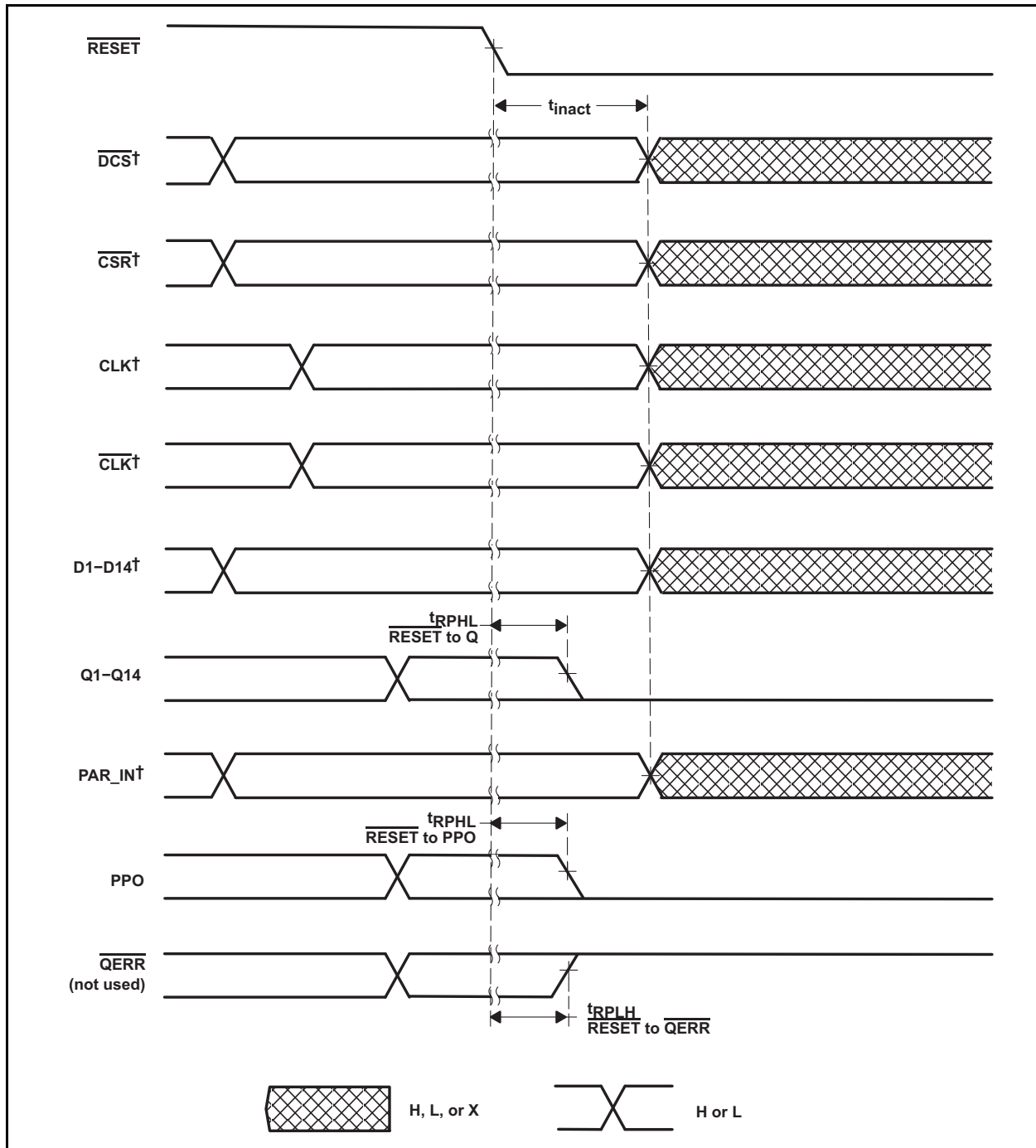


Figure 14 — Timing Diagram for the First SSTUB32866 (1:2 Register-A Configuration) Device Used in Pair; $C0 = 0$, $C1 = 1$; $\overline{\text{RESET}}$ Switches from H to L

† After $\overline{\text{RESET}}$ is switched from high to low, all data and clock inputs signals must be held at valid logic levels (not floating) for a minimum time of $t_{\text{INACT max}}$

2.7 Register Timing (cont'd)

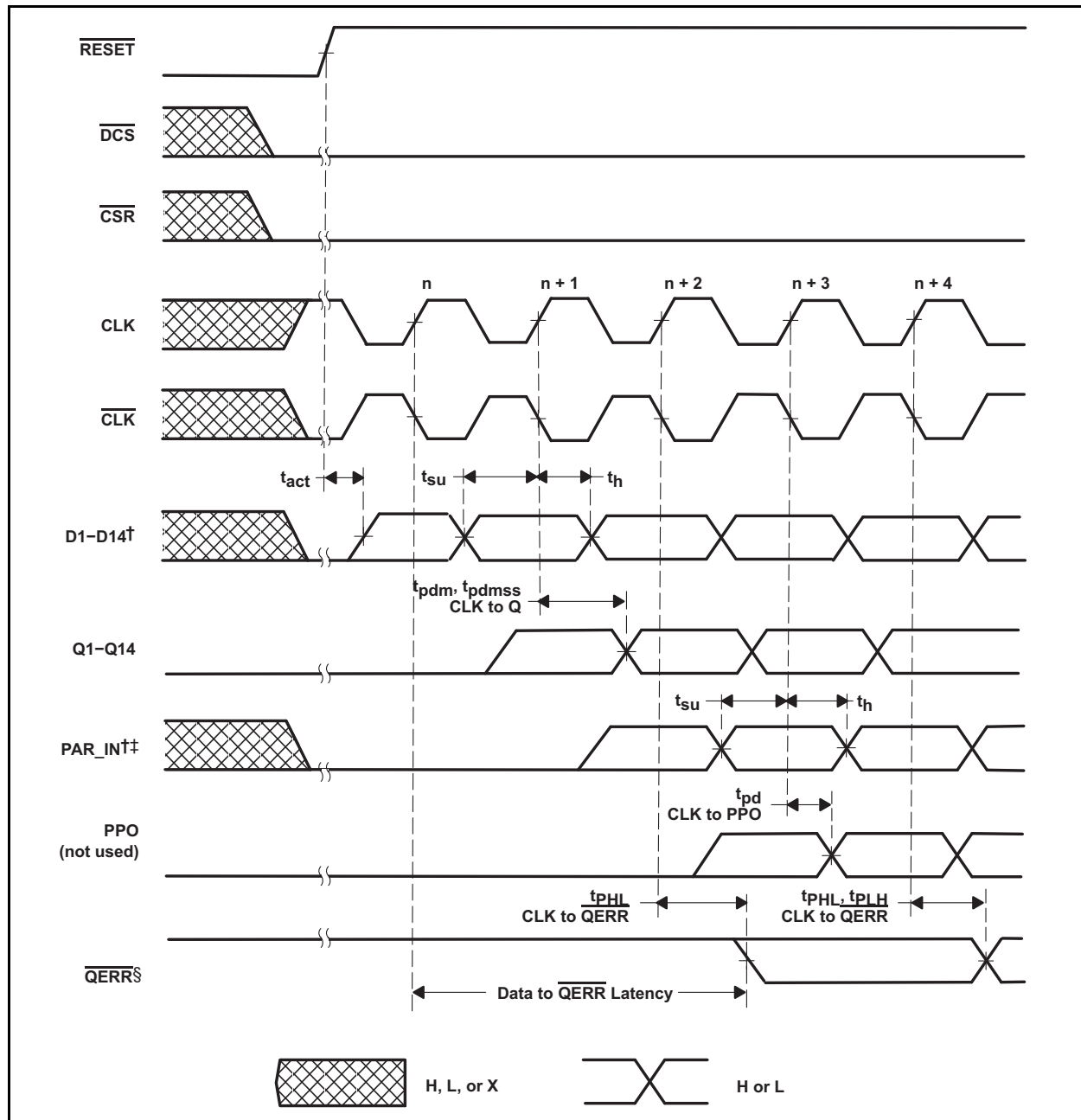


Figure 15 — Timing Diagram for the Second SSTUB32866 (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1; RESET Switches from L to H

† After \overline{RESET} is switched from low to high, if $\overline{DCS0}$ or $\overline{DCS1}$ are held Low then all data and $\overline{PAR_IN}$ input signals must be held Low for a minimum time of t_{ACT} max to avoid false error. If $\overline{DCS0}$ or $\overline{DCS1}$ are held high then all data and $\overline{PAR_IN}$ input signals must be held at valid logic levels for a minimum time of t_{ACT} max, to avoid false error.

‡ $\overline{PAR_IN}$ is driven from PPO of the first SSTUB32866 device

§ If the data is clocked in on the n clock pulse, and $\overline{PAR_IN}$ is clocked in at n+2, the \overline{QERR} output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse.

2.7 Register Timing (cont'd)

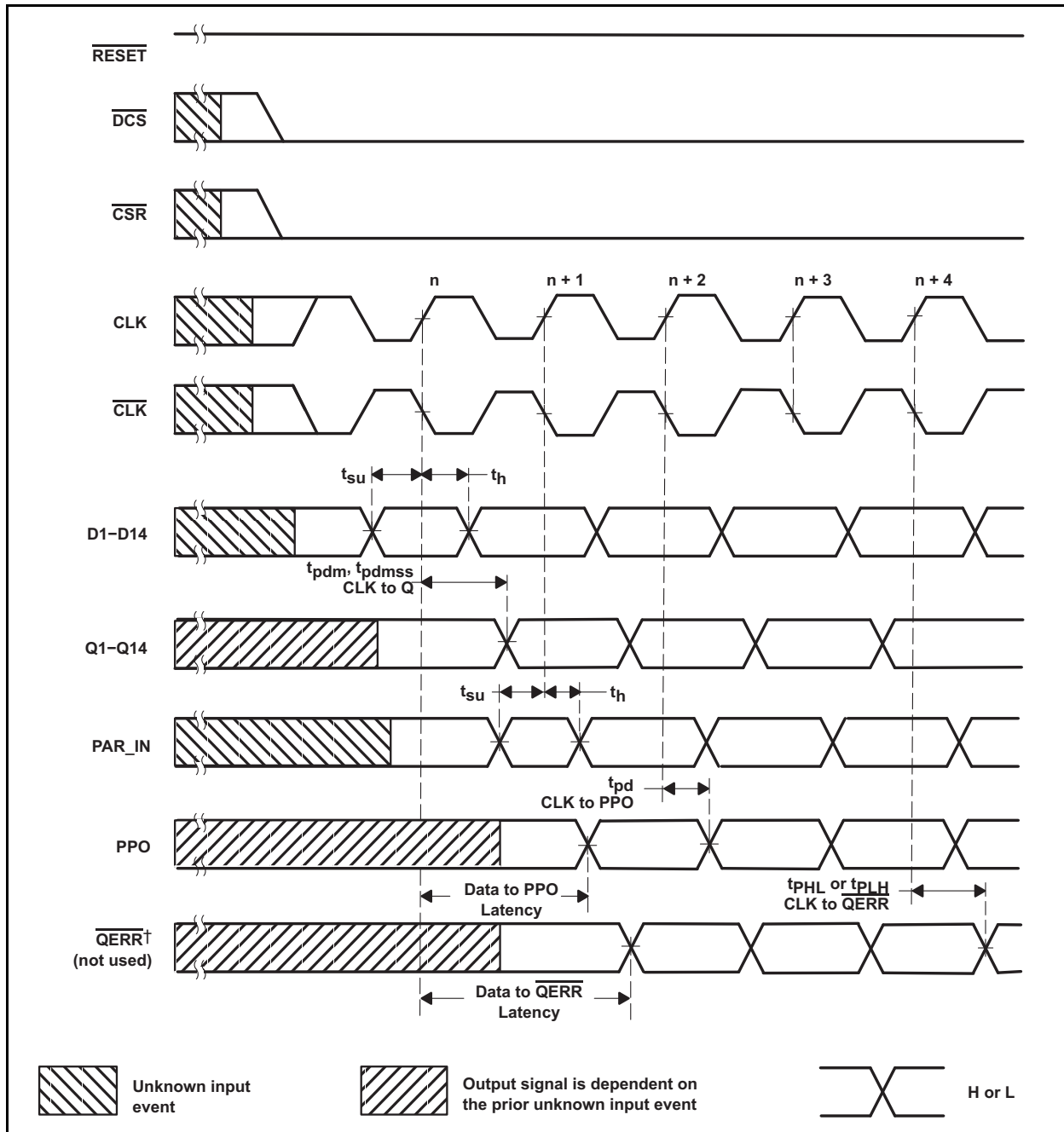


Figure 16 — Timing Diagram for the Second SSTUB32866 (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1; RESET Being Held HIGH

† PAR_IN is driven from PPO of the first SSTUB32866 device

‡ If the data is clocked in on the n clock pulse, and PAR_IN is clocked in at n+2, the QERR output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse. If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low.

2.7 Register Timing (cont'd)

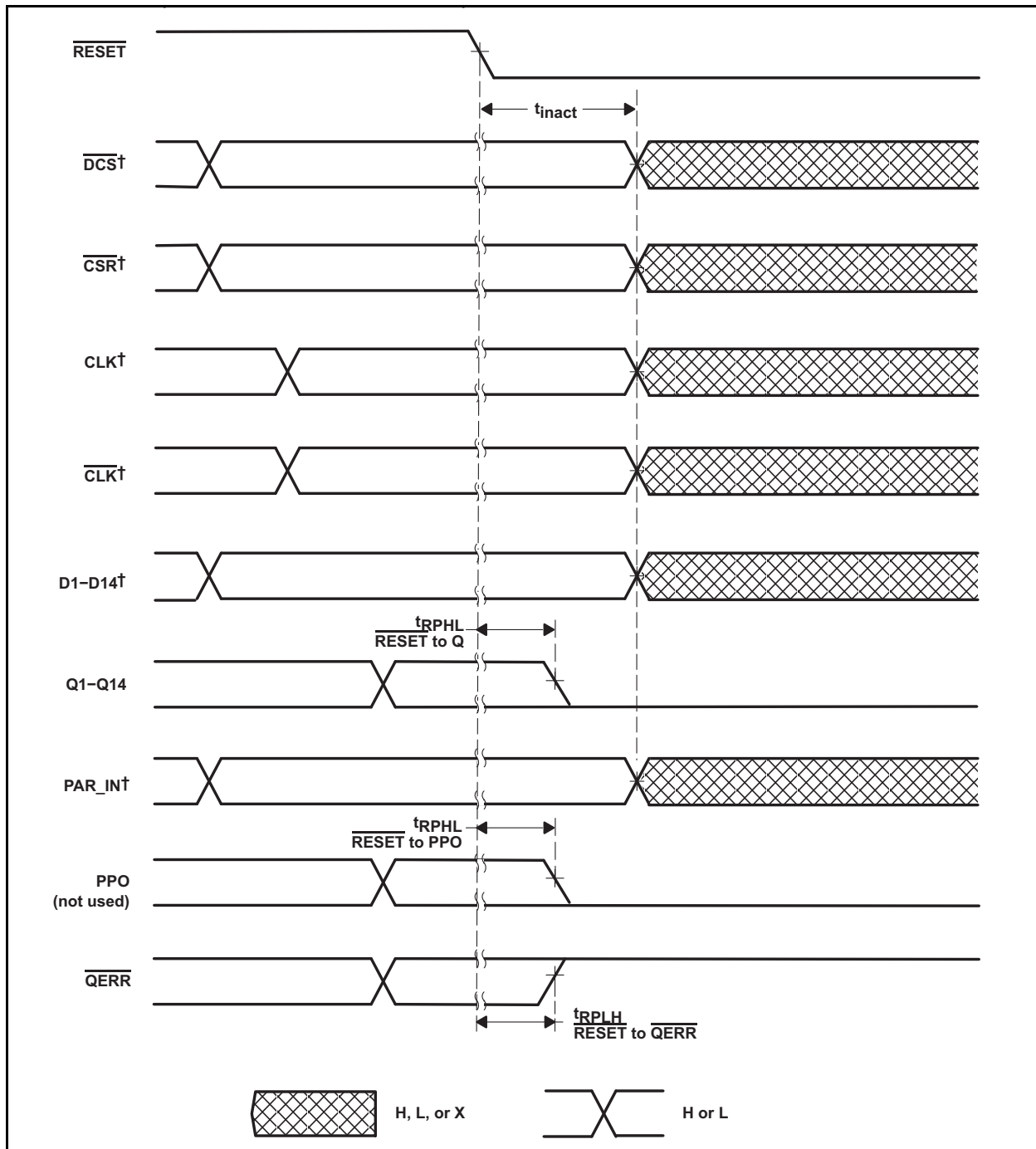


Figure 17 — Timing Diagram for the Second SSTUB32866 (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1; RESET Switches from H to L

† After $\overline{\text{RESET}}$ is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of $t_{INACT\ max}$

2.7 Register Timing (cont'd)

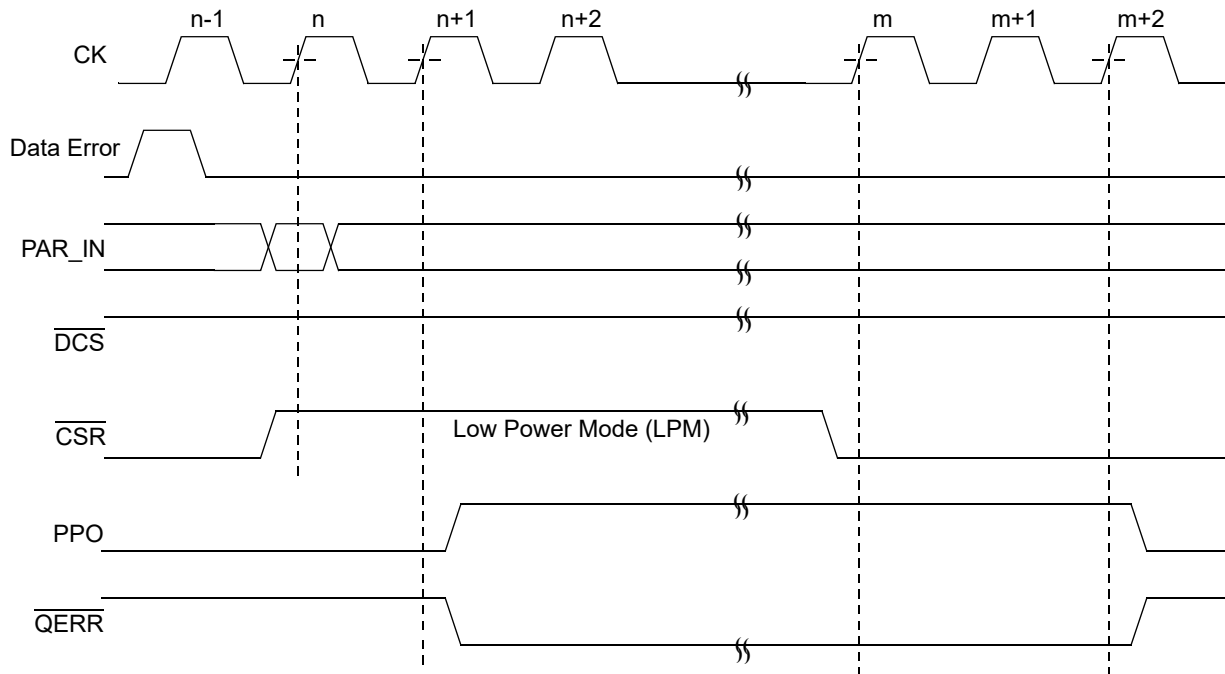


Figure 18 — 1:1 Mode, Data Error Occurs at (n-1), LPM Occurs at n

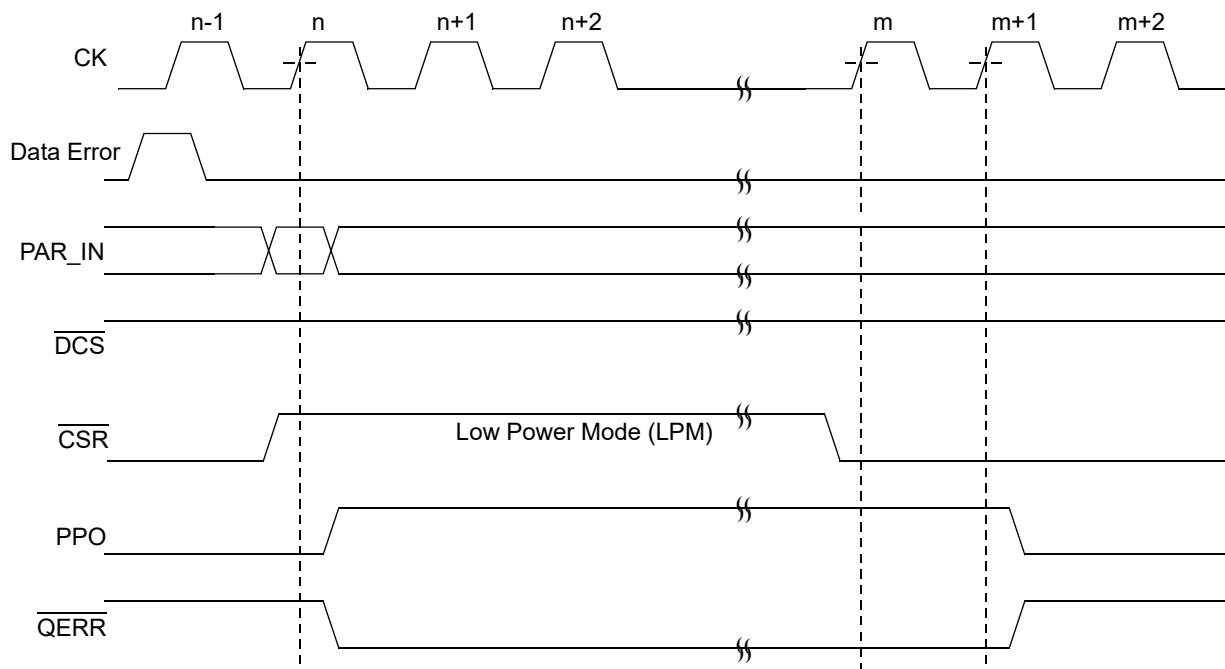
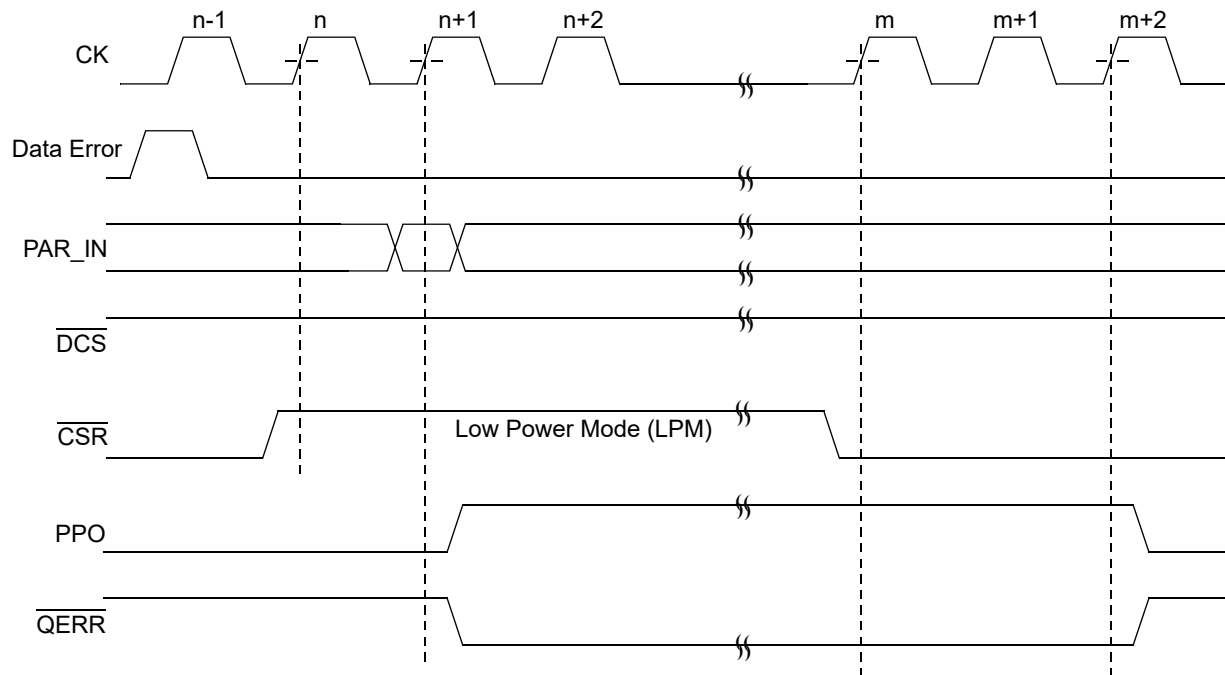


Figure 19 — 1:2A Mode, Data Error Occurs at (n-1), LPM Occurs at n

2.7 Register Timing (cont'd)**Figure 20 — 1:2B Mode, Data Error Occurs at (n-1), LPM Occurs at n**

2.7 Register Timing (cont'd)

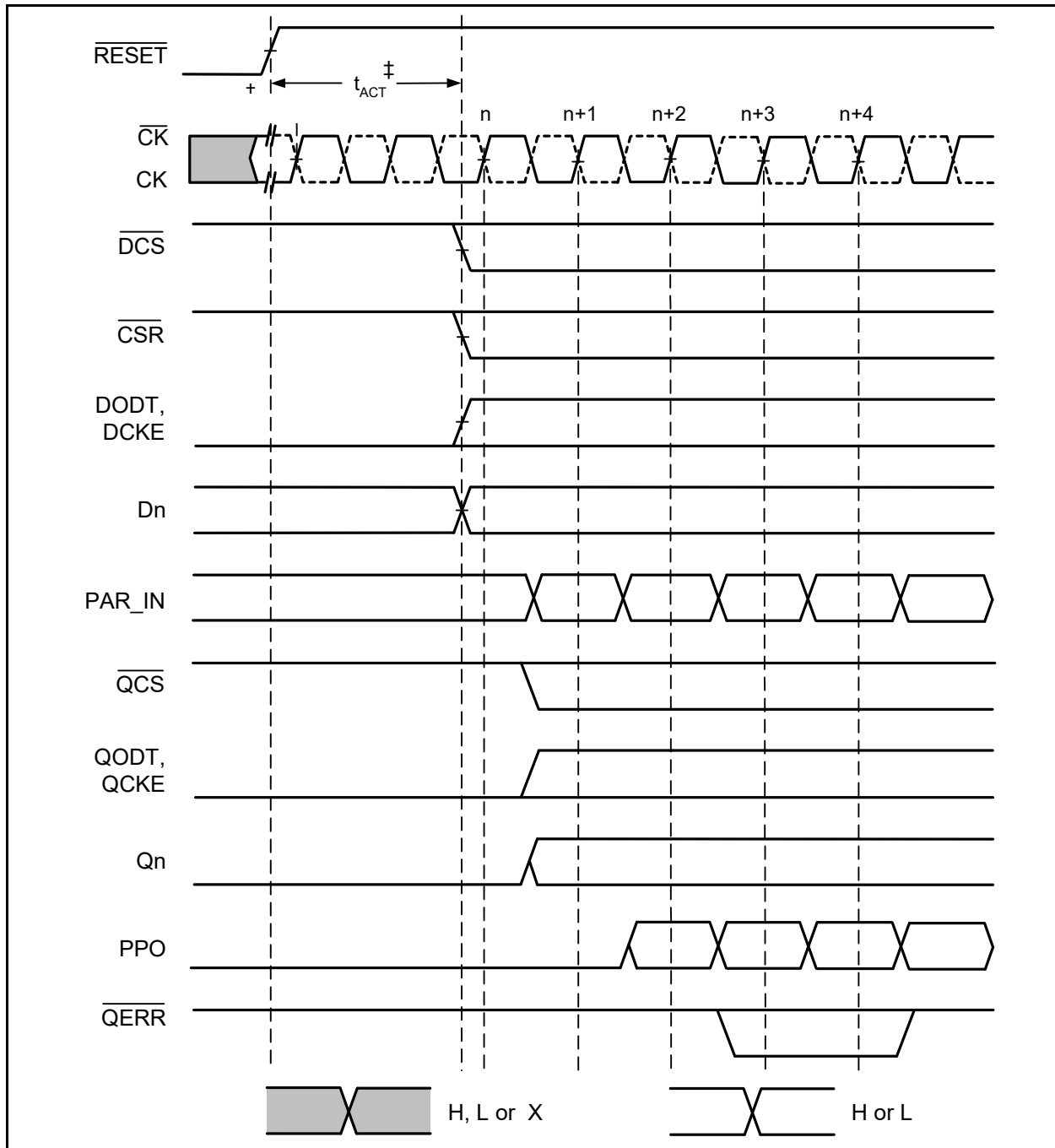


Figure 21 — Timing Diagram For Register Used As A Single Device; C0=0, C1=0; During Start-up when Data Inputs are LOW or HIGH (RESET Switches from L to H)

‡

After $\overline{\text{RESET}}$ is switched from low to high, $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ must be held HIGH, DODT and DCKE must be held LOW, and all other inputs must remain stable either LOW or HIGH (not floating) for a minimum time of $t_{ACT \text{ max}}$.

2.7 Register Timing (cont'd)

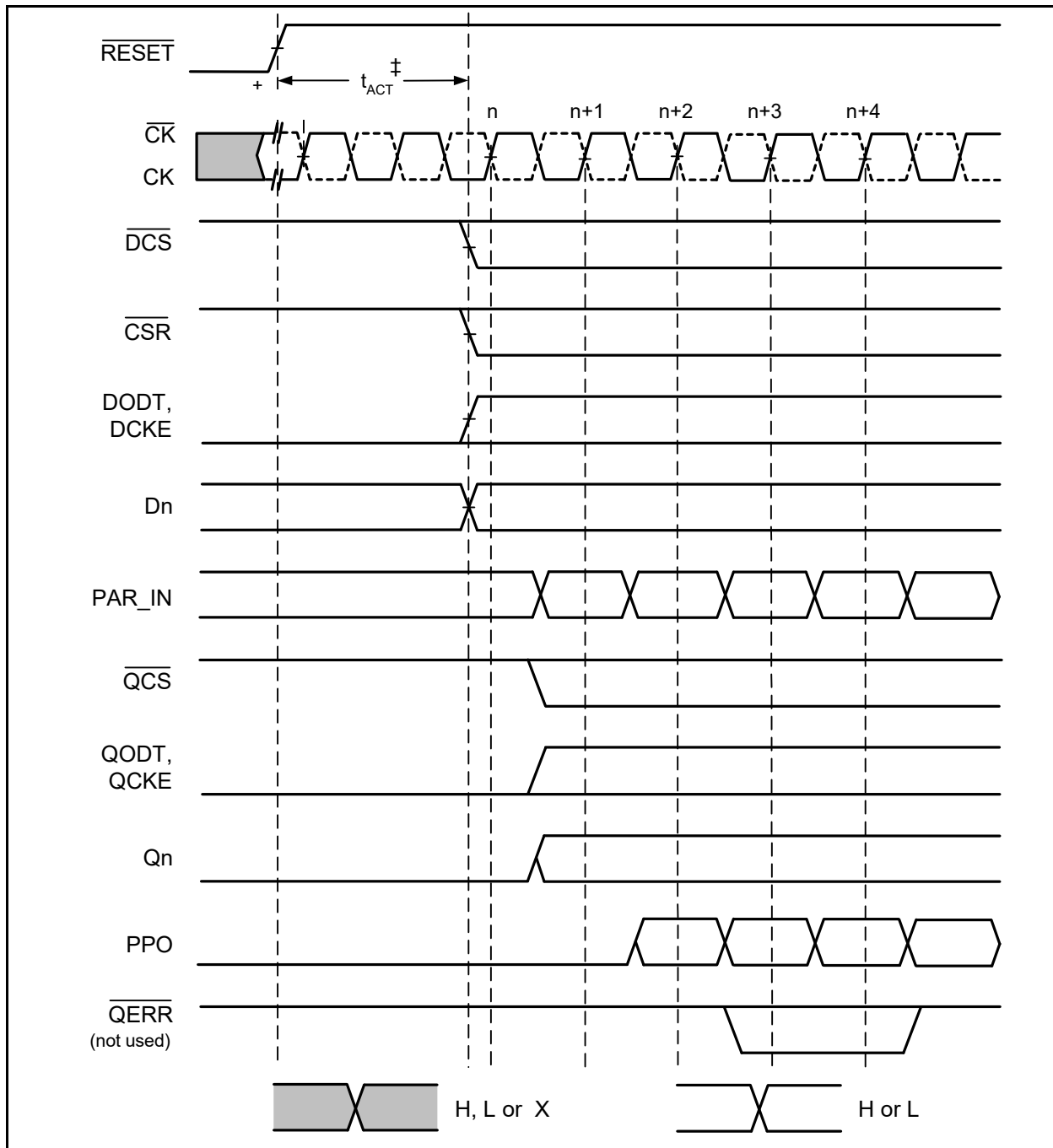


Figure 22 — Timing Diagram for First Device (1:2 Register-A Configuration) Used in a Pair; C0=0, C1=1; During Start-up When Data Inputs are LOW or HIGH, (RESET Switches from L to H)

‡

After $\overline{\text{RESET}}$ is switched from low to high, $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ must be held HIGH, DODT0 and DCKE must be held LOW, and all other inputs must remain stable either LOW or HIGH (not floating) for a minimum time of t_{ACT} max.

2.7 Register Timing (cont'd)

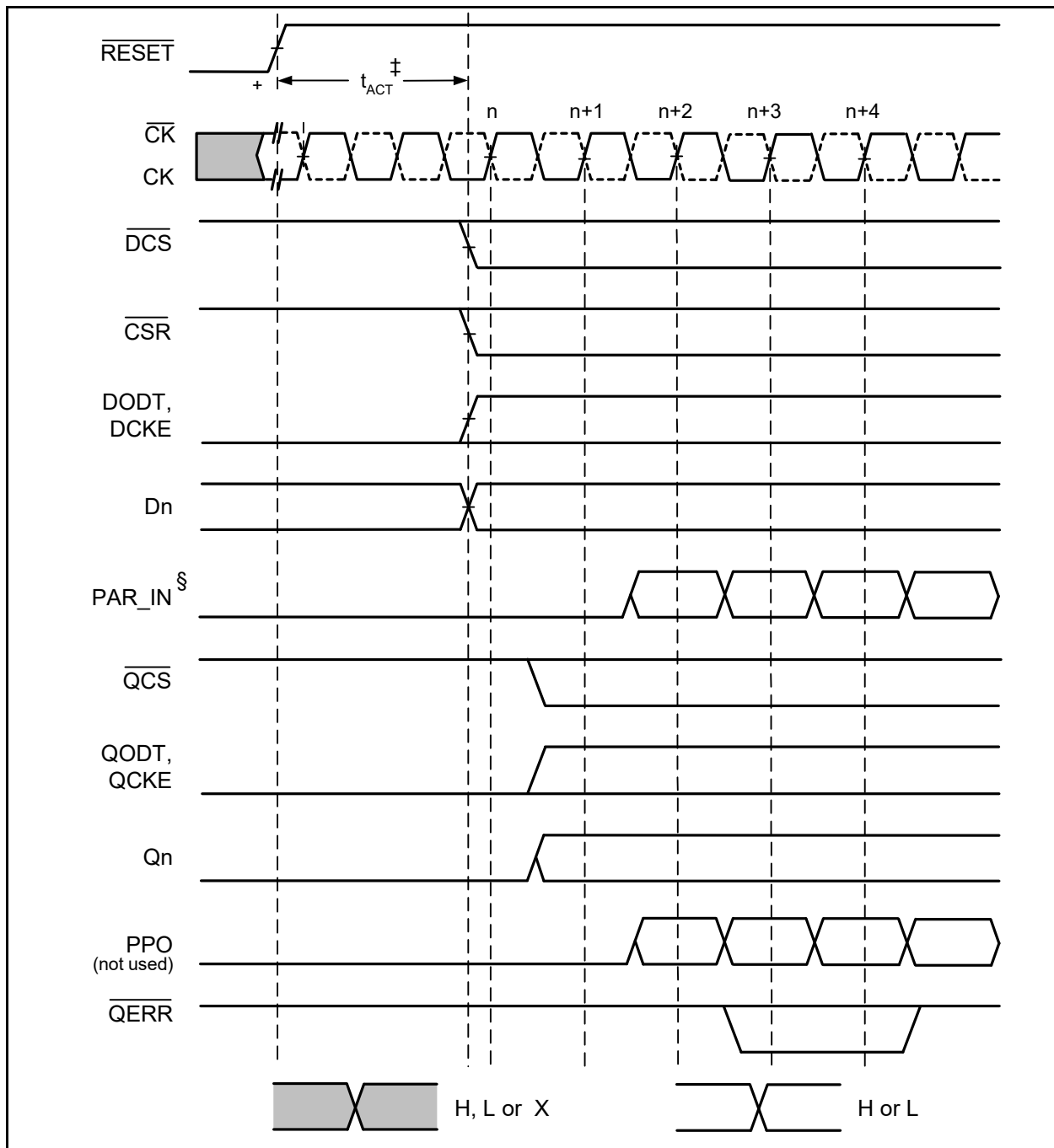


Figure 23 — Timing Diagram for Second Device (1:2 Register-B Configuration) Used in a Pair; C0=1, C1=1; During Start-up When Data Inputs are LOW or HIGH, (RESET Switches from L to H)

‡ After $\overline{\text{RESET}}$ is switched from low to high, $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ must be held HIGH, DODT and DCKE must be held LOW, and all other inputs must remain stable either LOW or HIGH (not floating) for a minimum time of t_{ACT} max.

§ PAR_IN is driven from PPO of the first SSTUB32866 device

2.8 Absolute Maximum Ratings

Table 5 — Absolute Maximum Ratings Over Operating Free-air Temperature Range (see Note 1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		−0.5	+2.5	V
V_I	Receiver input voltage	(See Notes 2 and 3)	−0.5	+2.5	V
V_O	Driver output voltage	(See Notes 2 and 3)	−0.5	$V_{DD} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$		±50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$		±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$		±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin			±100	mA
T_{stg}	Storage temperature		−65	+150	°C
NOTE 1	Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.				
NOTE 2	The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.				
NOTE 3	This value is limited to 2.5 V maximum.				

Symbol	Parameter		Min	Nom	Max	Unit
V _{DD}	Supply voltage		1.7	-	1.9	V
V _{REF}	Reference voltage		$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V _{TT}	Termination voltage		V _{REF} – 40 mV	V _{REF}	V _{REF} + 40 mV	V
V _I	Input voltage		0	-	V _{DD}	V
V _{IH}	AC HIGH-level input voltage	Data, \overline{CSR} , PAR_IN inputs	V _{REF} + 250 mV	-	-	V
V _{IL}	AC LOW-level input voltage		-	-	V _{REF} – 250 mV	V
V _{IH}	DC HIGH-level input voltage		V _{REF} + 125 mV	-	-	V
V _{IL}	DC LOW-level input voltage		-	-	V _{REF} – 125 mV	V
V _{IH}	HIGH-level input voltage	\overline{RESET} , Cn	$0.65 \times V_{DD}$	-	-	V
V _{IL}	LOW-level input voltage		-	-	$0.35 \times V_{DD}$	V
V _{ICR}	Common-mode input voltage range	CK, \overline{CK}	0.675	-	1.125	V
V _{ID}	Differential input voltage		600	-	-	mV
I _{OH}	HIGH-level output current		-	-	-6	mA
I _{OL}	LOW-level output current		-	-	6	mA
I _{ERROL}	\overline{QERR} LOW-level output current		25	-	-	mA
T _{amb}	Operating ambient temperature in free-air		0	-	+70	°C
NOTE	The \overline{RESET} and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless \overline{RESET} is LOW.					

Table 7 — Electrical Characteristics Over Recommended Operating Free-air Temperature Range

NOTE 1 The vendor must supply this value for full device description.

2.11 Timing Requirements

Table 8 — Timing Requirements Over Recommended Operating Free-air Temperature Range (see Figure 6)

Symbol	Parameter		Min	Max	Unit
f_{clock}	Clock frequency		-	410	MHz
t_W	Pulse duration, CK, $\overline{\text{CK}}$ HIGH or LOW		1	-	ns
t_{ACT}	Differential inputs active time (See Notes 1 and 2)		-	10	ns
t_{INACT}	Differential inputs inactive time (See Notes 1 and 3)		-	15	ns
t_{SU}	Setup time	$\overline{\text{DCS}}$ before CK \uparrow , $\overline{\text{CK}}$ \downarrow , for $\overline{\text{CSR}}$ high $\overline{\text{CSR}}$ before CK \uparrow , $\overline{\text{CK}}$ \downarrow , for $\overline{\text{DCS}}$ high	0.6	-	ns
	Setup time	$\overline{\text{DCS}}$ before CK \uparrow , $\overline{\text{CK}}$ \downarrow , for $\overline{\text{CSR}}$ low	0.5	-	ns
	Setup time	DODT, DCKE and data before CK \uparrow , $\overline{\text{CK}}$ \downarrow	0.5	-	ns
	Setup time	PAR_IN before CK \uparrow , $\overline{\text{CK}}$ \downarrow	0.5	-	ns
t_{H}	Hold time	$\overline{\text{DCS}}$, DODT, DCKE and data after CK \uparrow , $\overline{\text{CK}}$ \downarrow	0.4	-	ns
	Hold time	PAR_IN after CK \uparrow , $\overline{\text{CK}}$ \downarrow	0.4	-	ns
NOTE 1	This parameter is not necessarily production tested.				
NOTE 2	V_{REF} must be held at a valid input voltage level and data inputs must be held at valid logic levels for a minimum time of t_{ACT} (max) after $\overline{\text{RESET}}$ is taken high.				
NOTE 3	V_{REF} , Data and clock inputs must be held at valid voltage levels (not floating) a minimum time of t_{INACT} (max) after $\overline{\text{RESET}}$ is taken low.				

2.12 AC Specifications

Table 9 — Switching Characteristics Over Recommended Operating Free-air Temperature Range (Unless Otherwise Noted) (see Clause 3.1)

Symbol	Parameter	Measurement Conditions	Min	Max	Unit
f_{MAX}	Maximum input clock frequency		410	-	MHz
t_{pdm}	Propagation delay, single bit switching	From CK \uparrow and $\overline{\text{CK}}$ \downarrow to Qn (see Note 1)	1.1	1.5	ns
t_{pd}	Propagation delay	From CK \uparrow and $\overline{\text{CK}}$ \downarrow to PPO	0.5	1.7	ns
t_{LH}	Low-to-high propagation delay	From CK \uparrow and $\overline{\text{CK}}$ \downarrow to $\overline{\text{QERR}}$	1.2	3	ns
t_{HL}	High-to-low propagation delay		1	2.4	ns
t_{pDMSS}	Propagation delay, simultaneous switching	From CK \uparrow and $\overline{\text{CK}}$ \downarrow to Qn (See Notes 1 and 2)	-	1.6	ns
t_{PHL}	High-to-low propagation delay	From $\overline{\text{RESET}}$ \downarrow to Qn \downarrow	-	3	ns
t_{PHL}	High-to-low propagation delay	From $\overline{\text{RESET}}$ \downarrow to PPO \downarrow	-	3	ns
t_{PLH}	Low-to-high propagation delay	From $\overline{\text{RESET}}$ \downarrow to $\overline{\text{QERR}}$ \uparrow	-	3	ns
NOTE 1	Includes 350 ps of test-load transmission line delay.				
NOTE 2	This parameter is not necessarily production tested.				

2.13 Output Buffer Characteristics

Table 10 — Output Edge Rates Over Recommended Operating Free-air Temperature Range (see Clause 3.2)

Symbol	Parameter	Measurement Conditions	Min	Max	Unit
dV/dt _r	rising edge slew rate	From 20% to 80%	1	4	V/ns
dV/dt _f	falling edge slew rate	From 80% to 20%	1	4	V/ns
dV/dt _Δ ¹	absolute difference between dV/dt _r and dV/dt _f	From 20% or 80% to 80% or 20%	-	1	V/ns
NOTE 1 Difference between dV/dt _r (rising edge rate) and dV/dt _f (falling edge rate).					

2.14 Output Buffer Overshoot/Undershoot

This register is - among other applications - intended for use in the JEDEC reference designs as defined in JESD21-C, DDR2 Registered DIMM Design Standard. It is designed and characterized to produce overshoots/undershoots less than indicated in the table below, to comply with DDR2 SDRAM overshoot/undershoot requirements under worst case DRAM loading conditions (Min or Max), over DIMM operating conditions, and within the recommend operating conditions of the register listed in Table 5.

Table 11 — Output Overshoot/Undershoot Over Recommended Operating Free-air Temperature Range

DIMM Design Specification	Reference Design	Speed bin	Overshoot (above VDD) max ¹	Undershoot (below GND) min ¹
e.g., DDR2 Registered DIMM Design Specification Rev 2.0	e.g., F0	e.g., PC2-4200	e.g., 0.5 V	e.g., -0.5 V
...
...
NOTE 1 This value is verified by design and characterization, and may not be subject to production test				

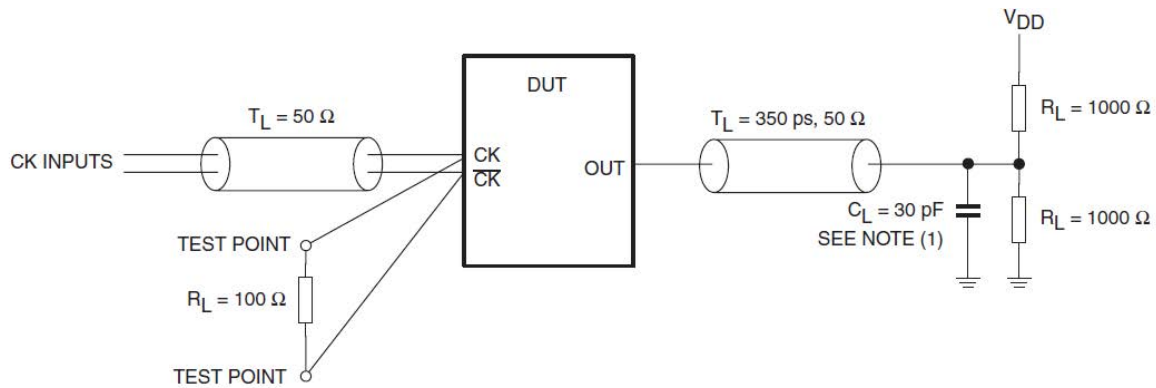
Register vendors are expected to supply the data in this table for the intended applications in their respective data sheets or in other suitable form.

3 Test Circuits and Switching Waveforms

3.1 Parameter Measurement Information for Data Output Load Circuit ($V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$)

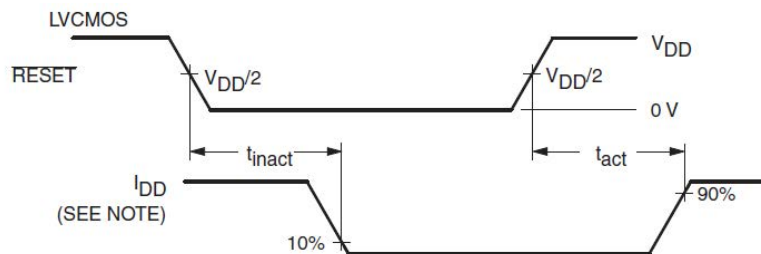
All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$;
 $Z_o = 50 \Omega$; input slew rate = $1 \text{ V/ns} \pm 20\%$, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



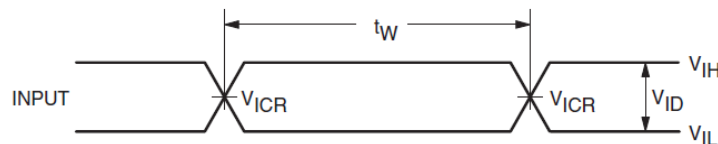
NOTE (1) C_L includes probe and jig capacitance.

Figure 24 — Load Circuit, Data Output Measurements



NOTE I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_O = 0 \text{ mA}$.

Figure 25 — Voltage and Current Waveforms; Inputs Active and Inactive Times



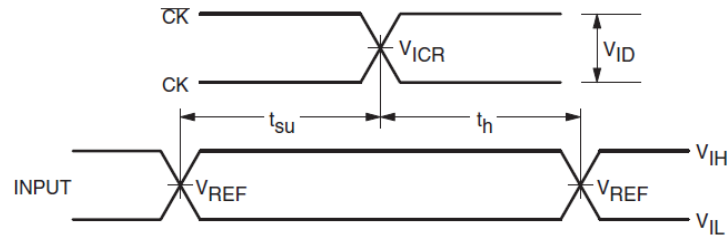
NOTE 1 $V_{ID} = 600 \text{ mV}$

NOTE 2 $V_{IH} = V_{REF} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVTMOS inputs.

NOTE 3 $V_{IL} = V_{REF} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVTMOS inputs.

Figure 26 — Voltage Waveforms; Pulse Duration

3.1 Parameter Measurement Information (cont'd)



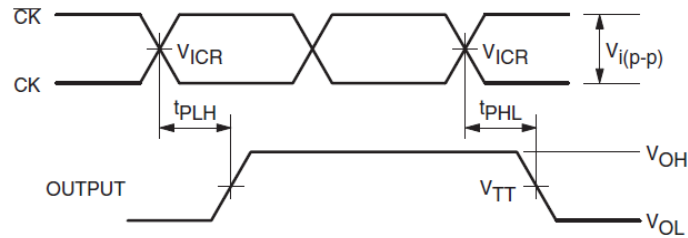
NOTE 1 $V_{ID} = 600 \text{ mV}$

NOTE 2 $V_{REF} = V_{DD}/2$

NOTE 3 $V_{IH} = V_{REF} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS inputs.

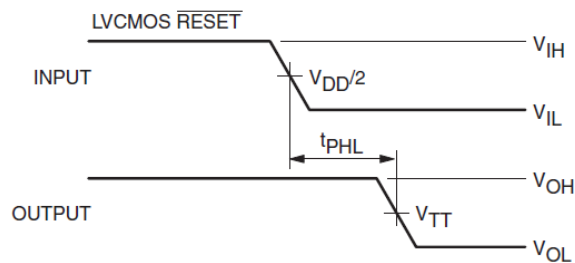
NOTE 4 $V_{IL} = V_{REF} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVC MOS inputs.

Figure 27 — Voltage Waveforms; Set-up and Hold Times



NOTE t_{PLH} and t_{PHL} are the same as t_{PD} .

Figure 28 — Voltage Waveforms; Propagation Delay Times



NOTE 1 t_{PLH} and t_{PHL} are the same as t_{PD} .

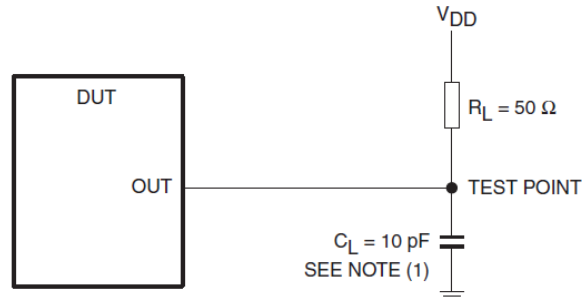
NOTE 2 $V_{IH} = V_{REF} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS inputs.

NOTE 3 $V_{IL} = V_{REF} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVC MOS inputs.

Figure 29 — Voltage Waveforms; Propagation Delay Times

3.2 Data Output Slew-rate Measurement Information ($V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$)

All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$; $Z_o = 50 \Omega$; input slew rate = $1 \text{ V/ns} \pm 20\%$, unless otherwise specified.



NOTE 1 C_L includes probe and jig capacitance.

Figure 30 — Load Circuit, HIGH-to-LOW Slew Measurement

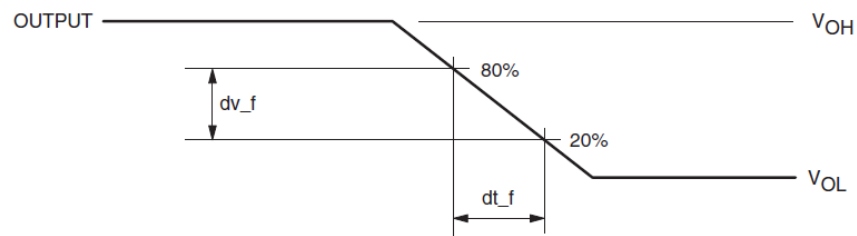
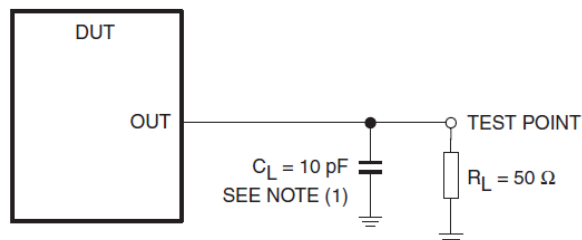


Figure 31 — Voltage waveforms, HIGH-to-LOW Slew Rate Measurement



NOTE 1 C_L includes probe and jig capacitance.

Figure 32 — Load Circuit, LOW-to-HIGH Slew Measurement

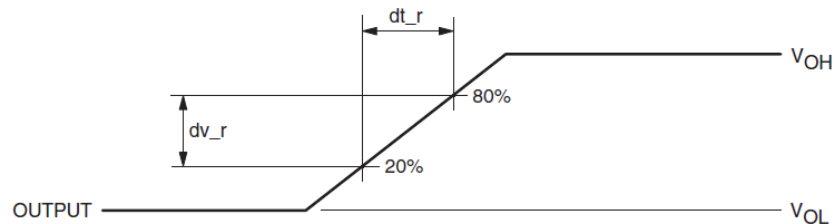
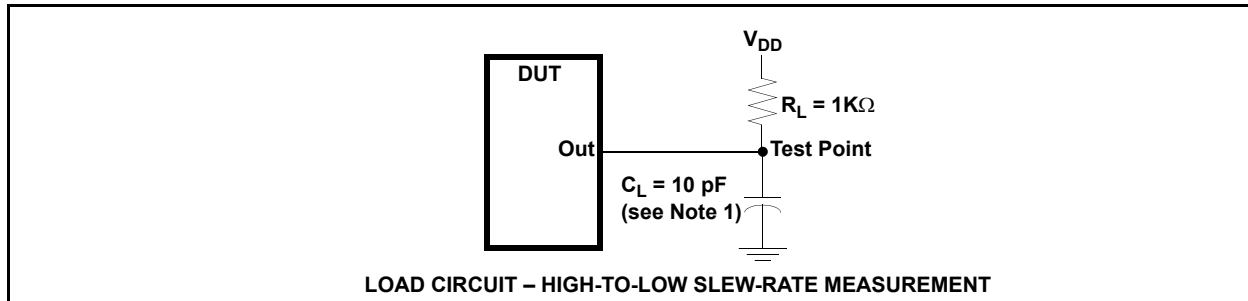


Figure 33 — Voltage Waveforms, LOW-to-HIGH Slew Rate Measurement

3.3 Error Output Load Circuit and Voltage Measurement Information ($V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$)

All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$; $Z_o = 50 \Omega$; input slew rate = $1 \text{ V/ns} \pm 20\%$, unless otherwise specified.



NOTE 1 C_L includes probe and jig capacitance.

Figure 34 — Load Circuit, Error Output Measurements

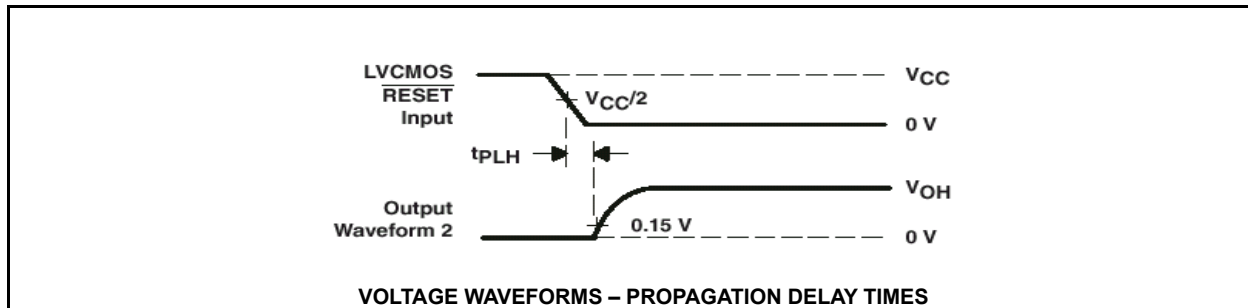


Figure 35 — Voltage Waveforms, Open-drain Output LOW-to-HIGH Transition Time with Respect to Reset Input

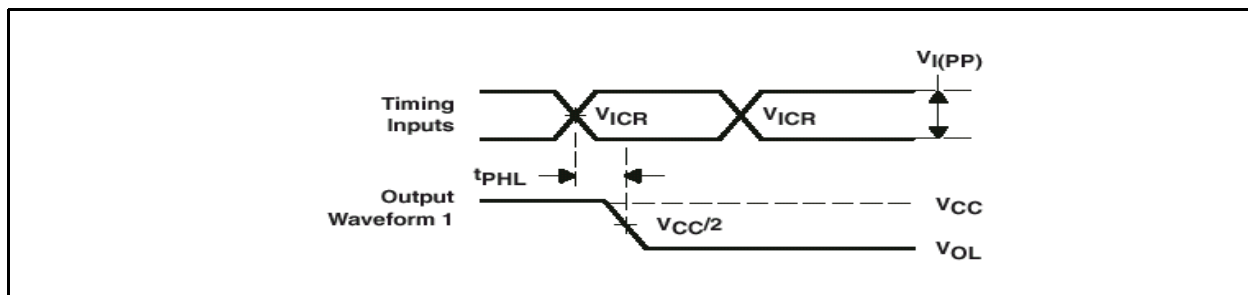


Figure 36 — Voltage Waveforms, Open-drain Output HIGH-to-LOW Transition Time with Respect to Clock Inputs

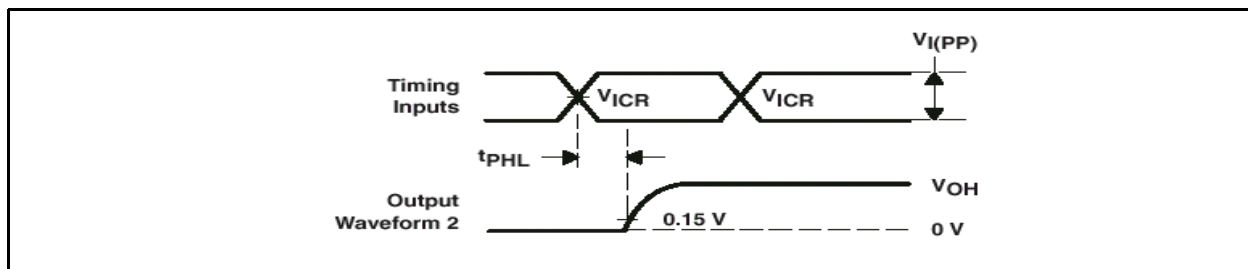
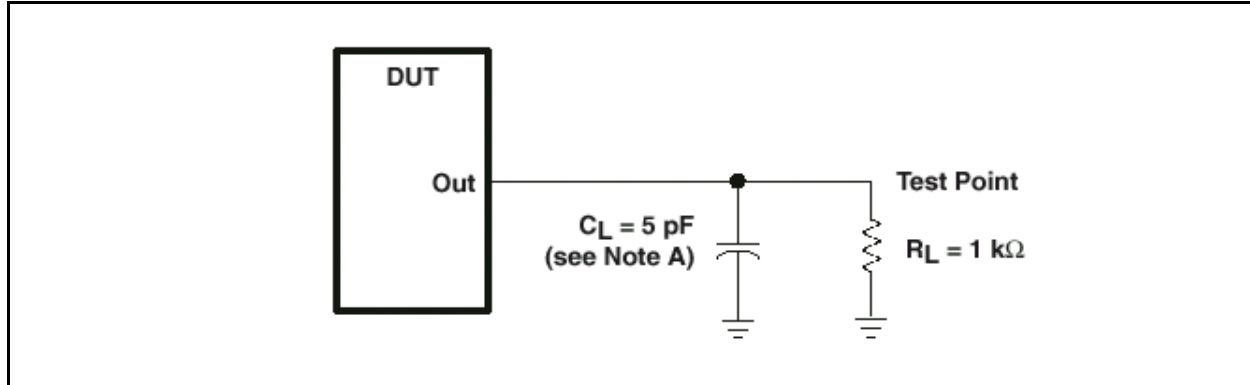


Figure 37 — Voltage Waveforms, Open-drain Output LOW-to-HIGH Transition Time with Respect to Clock Inputs

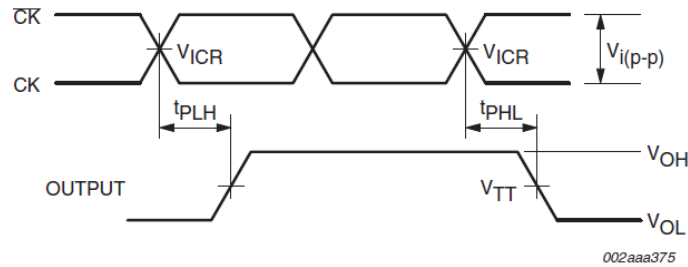
3.4 Partial-parity-out Load Circuit and Voltage Measurement Information ($V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$)

All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$; $Z_o = 50 \Omega$; input slew rate = $1 \text{ V/ns} \pm 20\%$, unless otherwise specified.



NOTE A C_L includes probe and jig capacitance.

Figure 38 — Partial-parity-out Load Circuit

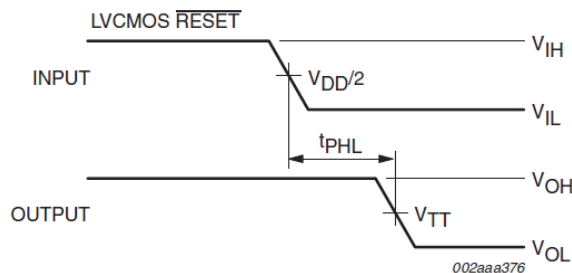


NOTE 1 $V_{TT} = V_{DD}/2$

NOTE 2 t_{PLH} and t_{PHL} are the same as t_{PD} .

NOTE 3 $V_{i(pp)} = 600 \text{ mV}$

Figure 39 — Partial-parity-out Voltage Waveforms; Propagation Delay Times with Respect to Clock Inputs



NOTE 1 $V_{TT} = V_{DD}/2$

NOTE 2 t_{PLH} and t_{PHL} are the same as t_{PD} .

NOTE 3 $V_{IH} = V_{REF} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS inputs.

NOTE 4 $V_{IL} = V_{REF} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVC MOS inputs.

Figure 40 — Partial-parity-out Voltage Waveforms; Propagation Delay Times with Respect to Reset Input

4 Reference to Other Applicable JEDEC Standards and Publications

- JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*.
- JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices*.
- JESD8-7, *1.8V +/- 0.15V (Normal Range), and 1.2 - 1.95V (Wide Range) Power Supply Voltage and Interface for Nonterminated Digital Integrated Circuits*.
- JESD8-15, *Stub Series Terminated Logic for 1.8 V (SSTL_18)*.
- JESD21-C, *Configuration for Solid State Memories*.
- JESD82-7, *Definition of the SSTU32864 1.8 V Configurable Registered Buffer for DDR2 RDIMM Applications*.
- JESD82-9, *Definition of the SSTU32865 1.8 V Registered Buffer with Parity for 2R x 4 DDR2 RDIMM Applications*.

5 Annex A - (Informative) Differences between JESD82-25.01 and JESD82-25

- Terminology update on Table 1, changed “Master clock” to “Main clock”
- Reformatted the cover page to JEDEC standard
- Updated the JEDEC logo on front and back pages
- Removed the EIA logo from front page
- Moved table notes to inside of tables
- Added the JEDEC Standard Improvement Form
- Added Table of Contents, List of Tables, and List of Figures



Standard Improvement Form**JEDEC Standard JESD82-25.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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Suite 240 South
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause num- _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

Name: _____

Company: _____

Address: _____

City/State/Zip: _____

Phone: _____

E-mail: _____

Date: _____

